REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

No new matter has been introduced by any of the above amendments.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231, on November 12, 2002.

Pat Slaback
Name

Signature

VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS

39. (New) A system, comprising:

a memory device; and

a field programmable gate array, wherein the field programmable gate array comprises:

a logic fabric that includes a plurality of configurable logic blocks, switching blocks, and input/output blocks, wherein at least a portion of the logic fabric is configured as a first configured processor to perform a first fixed logic function, and at least a portion of the input/output blocks are coupled to the memory device;

a fixed logic processor embedded within the logic fabric; and

a first auxiliary processing interface that couples the first configured processor to perform the first fixed logic function to the fixed logic processor.

40. (New) The system of Claim 39, wherein the field programmable gate array further comprises:

a second fixed logic processor embedded within the logic fabric; and

a second auxiliary processing interface that couples the second fixed logic processor to the first configured processor to perform the first fixed logic function.

41. (New) The system of Claim 39, wherein:

in the field programmable gate array a second portion of the logic fabric is configured as a second configured processor to perform a second fixed logic function; and

the field programmable gate array further comprises a second auxiliary processing interface that couples the second configured processor to perform the second fixed logic function to the fixed logic processor.

42. (New) The system of Claim 39, wherein:

in the field programmable gate array a second portion of the logic fabric is configured as a second configured processor to perform a second fixed logic function; and

the field programmable gate array further comprises addressing means for enabling the fixed logic processor to address the first configured processor to perform the first fixed logic function or the second configured processor to perform the second fixed logic function.

43. (New) The system of Claim 39, wherein:

in the field programmable gate array a second portion of the logic fabric is configured as a second configured processor to perform a second fixed logic function; and

the field programmable gate array further comprises:

a second fixed logic processor embedded within the logic fabric; and

a second auxiliary processing interface that couples the second fixed logic processor to the second configured processor to perform the second fixed logic function.